

In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the new mandatory amendment format.

1 1. (Previously Presented) A method comprising:
2 receiving real-time analog data at a personal computer implementing a general
3 purpose operating system;
4 generating a real-time event at the personal computer indicating a request to
5 process the real time data;
6 determining whether the real-time event has a higher priority than a first non-real
7 time event being processed at the personal computer; and
8 processing the real-time data if the real-time event has a higher priority than the
9 first non-real time event.

1 2. (Previously Presented) The method of claim 1 further comprising
2 continuing to process the first non-real time event if the real-time event does not have a
3 higher priority than the first event.

1 3. (Previously Presented) The method of claim 1 further comprising:
2 saving the state of the first non-real time event at the personal computer prior to
3 processing the real-time event; and
4 processing the first non-real time event after processing of the real-time event has
5 been completed.

1 4. (Previously Presented) The method of claim 1 further comprising:
2 receiving a second non-real time event while processing the real-time event; and

3 determining whether the second non-real time event has a higher priority than the
4 real-time event.

1 5. (Previously Presented) The method of claim 4 further comprising:
2 continuing the processing of the real-time event if the second non-real time event
3 does not have a higher priority than the real time event.

1 6. (Previously Presented) The method of claim 4 further comprising:
2 terminating the processing of the real-time event if the second non-real time event
3 has a higher priority; and
4 processing the second non-real time event.

1 7. (Currently Amended) A computer system comprising:
2 a chipset;
3 a bus coupled to the chipset; and
4 a central processing unit (CPU), coupled to the bus, to generate a real-time ~~events~~
5 event upon receiving real-time analog data at the computer system and to process the
6 real-time event ~~analog data~~ if the real-time event has a higher priority than a non-real-
7 time event.

1 8. (Previously Presented) The computer system of claim 7 wherein the CPU
2 comprises:
3 a timer to generate timing signals at predetermined time intervals; and
4 an event mechanism coupled to the timer to generate the real time events.

1 9. (Previously Presented) The computer system of claim 8 wherein the CPU
2 further comprises an event handler coupled to the event mechanism to process the real-
3 time events.

1 10. (Original) The computer system of claim 9 wherein the CPU further
2 comprises a register coupled to the event mechanism to store real-time data.

1 11. (Previously Presented) The computer system of claim 9 wherein the event
2 mechanism determines the relative priority between the real-time events and the non-real-
3 time events.

1 12. (Original) The computer system of claim 11 wherein the CPU further
2 comprises an analog to digital converter coupled to the register.

1 13. (Previously Presented) A central processing unit (CPU) comprising:
2 a timer to generate timing signals at predetermined time intervals;
3 an event mechanism coupled to the timer to generate real time events in response
4 to receiving the timing signals and real-time data; and
5 an event handler coupled to the event mechanism to process the real-time events
6 received from the event mechanism upon determining the relative priority between the
7 real-time events and non-real-time events.

1 14. (Previously Presented) The computer system of claim 13 wherein the CPU
2 further comprises a register coupled to the event mechanism to store real-time data.

1 15. (Previously Presented) The computer system of claim 14 wherein the event
2 handler verifies whether there is data stored in register upon detecting a real-time event
3 and determines the priority of the real-time event relative to other interrupts received.

1 16. (Previously Presented) The computer system of claim 14 wherein the CPU
2 further comprises an analog to digital converter coupled to the register.

1 17. (Previously Presented) The method of claim 1 wherein receiving the real-
2 time analog data comprises:
3 converting the real-time analog data to digital data; and
4 storing the digital data at a register.